Proceedings of DETC '04
2004 ASME Design Engineering Technical Conferences
and Computers and Information in Engineering Conference
September 28 – October 2, 2004, Salt Lake City, Utah

DETC2004/DTM-57338

FAILURE ANALYSIS IN SUBSYSTEM DESIGN FOR SPACE MISSIONS

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ABSTRACT

In order for the Function-Failure Design method to be applicable to modern conceptual design, the method needs to be extended from the mechanical domain to include the electrical domain as very few modern systems are purely mechanical in nature. Towards this goal, we supplement previous efforts describing a standardized vocabulary for mechanical failures by presenting the current state of an electrical and a mechanical failure mode taxonomy. Failure is defined in terms of the cause of the failure mode, the failure mode, and the effect of the failure mode that renders a mechanical, electrical, or electromechanical device incapable of satisfactorily performing its intended function under normal usage conditions. We utilize an elemental physics of failure approach to define *failure mode* and then use this definition and a variety of resources to develop the electrical failure modes presented in the taxonomy. The list of proposed electrical failure modes is tested against a set of NASA problem reports before being revised to include additional failure modes encountered in space applications. The resulting taxonomy is summarized in the form of 38 electrical failure modes organized into 13 categories. The final version of the mechanical and electrical failure mode taxonomy will be combined with a functional modeling approach to predict potential failures during the conceptual stages of design.

KEYWORDS

Electromechanical failure, Failure analysis, Failure mode taxonomy.

1. INTRODUCTION

Safety, performance and reliability are principal concerns of NASA missions. To deal with these concerns, there is a current push to include safety and risk assessment in the early stages of conceptual design. The insight needed to eliminate or reduce performance and safety problems can be achieved with a thorough understanding of potential failure modes and their causes.

In an analysis conducted in 1971 concerning failures in avionics systems due to environmental causes, part failures represented about 50% of the total failures whereas similar studies conducted in 1990 on systems which have been in the field operating for 2-8 years found the part failures to be negligible [1]. Improved design, manufacturing, and quality control procedures have led to more reliable electronic components. The trend away from the emphasis on failure of electronic components is the subject of a study reported by Boeing Commercial Airplane Group [1]. According to the report, the majority of failures can be prevented by thorough attention to system design, processes, and handling. Nearly 95% of the reported avionics systems failures in this 1992 study

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were caused by failures other than those associated with inherent component failures. Design and handling are undisputed and prevalent causes of avionics failures that need to be addressed. In addition, a failure margin of nearly 5% for electrical components is a necessary concern for high-risk aerospace applications.

Because the reported causes for component failures have not been consistent, dominant failure causes in one study are relatively insignificant in another which leads to a fairly large gap between the physics of failures and their effects at the electrical and logic levels [1, 2]. We seek to fill this gap by developing a *standardized* electrical and mechanical failure mode taxonomy to assist engineering designers in assessing both electrical and mechanical failure modes at the elemental physics-based level.

2. RELATED WORK

Engineers at NASA, as well as other design-intensive industries, use several supporting techniques including checklists, FMEA/FMECAs, and FTAs to anticipate potential failures [3]. Checklists are listings of relevant failure modes and mechanisms that are used as reminders to ensure designs have been adequately assessed. Checklists can be incomplete and lacking in all of the mechanisms leading to failure [3].

FMEA (failure modes and effects analysis) and FMECA (failure modes effects and criticality analysis) are bottom up approaches to failure analysis. These tools can be used to identify failure modes at a specific level, such as component or sub-assembly, before tracing the effect of the failure upward through the design hierarchy [4]. Ideally, the FMEA/FMECA would be performed when the system is first designed and repeated whenever any change is made to the design, but considering the tediousness and time required to perform a FMEA/FMECA, repeating the FMEA/FMECA process can be cost prohibitive [5]. As a result, the FMEA/FMECA is often performed late in the design cycle at a time when the cost of design changes or modifications can be enormous. Besides the FMEA/FMECA process being both tedious and time consuming, it also requires detailed expert knowledge of the structure and function of the system under consideration [6]. A fundamental weakness of the FMEA is the lack of a *standardized* language for failure modes [7]. FMEA/FMECAs currently use natural language to describe function, failure modes, failure effect, and failure cause. The use of natural language in these areas can lead to misunderstanding and ambiguity between team members and outside parties. In addition, user-based subjective rankings for the Risk Priority Number also increases variability.

FTA (fault tree analysis) is a top down approach to failure analysis. The FTA begins with an undesirable top level event and isolates possible causes at each successive lower level in the design hierarchy to arrive at the original cause(s) of each failure considered. FTA is more powerful than FMEA/FMECA in the sense that it forces the designers to consider all the causes of unacceptable top level events [3]. However, like the FMEA/FMECA, FTA is also subject to natural language and requires detailed expert knowledge of the structure and function of the system under consideration.

The FFD (function-failure design) method, developed by Tumer and Stone, utilizes both a standardized functional vocabulary and a standardized failure mode taxonomy [3, 8-11]. Like FMEA/FMECA and FTA, detailed knowledge and understanding of the systems being considered are required to *build* the FFD knowledge base, but the advantage is that once the information has been stored in this knowledge base, detailed information can then be retrieved and used by less experienced designers *during the earliest stages of conceptual design.*

2.1 Insight into the FFD Method

Although component information is not available in the conceptual design stage, functional information is available. The purpose of any design is to solve an overall function, and this overall function can be decomposed into numerous sub-functions in the form of a functional model. The functions in the functional model can then be linked to failure modes via the FFD method. Such function-failure information can be used to influence decisions during conceptual design.

The functional basis [10] and the failure mode taxonomy are needed to perform the FFD method, which is outlined in the following steps.

1. A black box model of the subsystem is created to identify the material, energy, and signal flows that flow into and out of the subsystem.
2. The functional model is created using functions from the functional basis and the Zen approach. Through the Zen approach (i.e., "be the flow"), the functions that must be performed on each flow as the flow progresses through the subsystem are identified. The functions are linked to form function chains, which in turn are combined to create the functional model.
3. The function-component (**EC**) matrix is generated using functions from the functional model and components from the bill of materials.
4. The component-failure (**CF**) matrix is populated using components from the functional model and failure modes from the failure mode taxonomy. If the goal is to link function to actual failure modes, then failure modes can be obtained from failure reports. If the goal is to link function to potential failure modes, then expert elicitation can be used to derive the failure modes.
5. The matrix multiplication of the **EC** and the **CF** matrices leads to the function-failure (**EF**) matrix, which links function to failure.
6. Aggregating many **EF** matrices together forms a database of function-failure information. The results of querying this database can be used to influence decisions during the earliest stages of conceptual design – at a time when the components that will be used to solve the function have not yet been determined.

Building the knowledge base will require a considerable time commitment, but once the knowledge base is available, it can be used in a matter of minutes. One important fact to understand is that the designer is not expected to create the knowledge base; the knowledge base is expected to be available to designers through an internet-based repository [12, 13] that is currently being developed. The designer would only need to know the functions their design is intended to perform in order to query the knowledge base to determine the actual or potential failure modes for each particular function.

In order for the Function-Failure Design method to be applicable to modern conceptual design, the method needs to be extended from the mechanical domain to the electrical domain. The first step in this process is to either locate or develop an electrical failure mode taxonomy similar to the existing mechanical failure mode taxonomy. Because a comprehensive list of electrical failure modes does not currently exist, at least to the authors' knowledge, such a taxonomy needs to be developed in order to be able to extend the FFD method to electrical systems.

3. RESEARCH APPROACH

The overall research approach consisted of three major steps. We first developed a clear definition of failure and failure mode. We then developed an electrical failure mode taxonomy based on the failure modes we found during literature review, personal experiences, and expert elicitation that could be defined using this concise definition of failure mode. The final step involved evaluating the proposed taxonomy against NASA spacecraft data and updating the taxonomy to include failure modes encountered in space applications.

3.1 Defining Failure

Failure can be a complicated concept. How can we define failure for use in a taxonomy such that the list is finite and useful? A taxonomy accounting for all possible failures to every kind of system would be infinite. Although one might be tempted to think of a failure as a mechanical device being obviously broken or an electrical device simply not working, most failures are more complicated and occur as a result of a complex set of interactions [14]. Collins defines mechanical failure as any change in the size, shape, or material properties of a structure, machine, or machine part that renders it incapable of satisfactorily performing its intended function [15]. Pecht and Ramappan define failure of an electronic system or device as the nonperformance or degraded performance under normal usage conditions [1].

The goal of this work is to extend the Collins classification of mechanical failure modes to include electrical failure modes. With this goal in mind, we first define the broad term *failure* as:

1. the cause of the failure mode,
2. the failure mode, and
3. the effect of the failure mode.

Using these three characteristics, we supplement previous efforts toward describing mechanical failures by Tumer, Stone et al. [11] which relied on work by Collins [15, 16] to define *electrical or mechanical* failure as the combination of the cause of the failure mode, the failure mode, and the effect of the failure mode that renders an electrical, mechanical or electromechanical device incapable of satisfactorily performing its intended function under normal usage conditions.

3.1.1 Failure Effect.

The effect of failure is what directly impacts the user and is, perhaps, the most appropriate starting point in our definitions of failure characteristics. To arrive at a definition for failure effect, we reviewed the individual definitions of Collins' mechanical failure modes [15] and observed that each mode had a common effect. The component was either broken into two or more pieces or was classified as no longer able to satisfactorily perform its intended function. From experience, we knew the result of most electrical failures is a short circuit, an open circuit, or a change in electrical component characteristics. Thus, we realized that a subset of effects result from all mechanical failures, and similarly, another subset of effects result from electrical failures. Combining these two subsets of effects into a single set, we claim the effects of all electrical, mechanical and electromechanical failures can be grouped into three high-level categories: a short or an open circuit, a component broken into two or more pieces, or a degraded performance such that the device is no longer able to satisfactorily perform its intended function. Intermittent failures and components that exhibit altered electrical characteristics fall in the latter category. An intermittent failure, which describes a failure that occurs from time to time, can be caused by numerous failure modes.

We formally define *failure effect* as physical evidence that a component or system has shorted or opened a circuit, broken into two or more pieces, or no longer performs its intended function at a satisfactory performance level.

Cause ➜ Failure Mode ➜ Effect

Figure 1. Failure mode is the link between failure cause and failure effect.

3.1.2 Failure Mode.

Next we turn to the second characteristic of failure – the failure mode. A notable discrepancy exists in the literature between the definitions of failure mode and failure mechanism. In some publications, the physical processes that lead to failure are termed failure mechanisms, and the effects of those failure mechanisms are termed failure modes [1, 2, 14, 17]. In spite of these plausible definitions of failure mechanism and failure mode, the widely accepted Failure Modes and Effects Analysis (FMEA) involves the investigation and assessment of the effects of possible failure modes on a system, and the effects of electrical failure modes are identified as shorts and open circuits [6]. If the effects of electrical failure are acknowledged as short or open circuits, then the failure mode is inferred to be the physical process that leads to the short or open circuit.

Stamatis defines failure mode as the physical description of the manner in which a failure occurs [18]. He further describes different levels of failure modes with the purpose of pursuing the root cause of the failure.

Schematically, we define failure mode as the link between failure cause and failure effect as shown in Figure 1. We adhere to the Collins [15, 16] classification and define *failure mode* as the physical process or processes that take place or combine to produce a failure effect. In general, failure modes are the physical, chemical, electrical, mechanical, electromagnetic, structural, thermal, or atomic processes that lead to failure.

3.1.3 Failure Cause.

Finally, we return to the initiating characteristic of failure – the failure cause. According to Dasgupta and Pecht [14], failure is caused by a lack of knowledge and/or indifference about user needs and desires, inattentive management, poor selection of materials or combinations of materials (structural defects), inadequate design, harsh environments, inappropriate manufacturing and assembly processes, lack of adequate technology, improper treatment by users, conditions during storage and field use, and poor control of quality. Essentially, all failures can be traced back to the design or manufacture of the materials used to make the device, the design or manufacture of the device itself, or the conditions in which the device is eventually used. Because our goal is a unified definition of failure mode, we formally define *failure cause* as the event that leads to the physical process or processes that take place or combine their effects to produce a failure mode.

3.2 Developing the Electrical Failure Mode Taxonomy

Previous work [11] has led to the extensive list of mechanical failure modes shown in Table 1. A variety of resources were investigated in an effort to derive a *comprehensive* electrical failure mode taxonomy. Literature review, expert elicitation from a NASA contractor, personal experiences, and our definition of failure mode were combined to ascertain the causes, failure modes, and effects that describe the manners in which electrical components fail at the elemental physics- based level. The resulting electrical failure mode taxonomy is presented in Table 2. The causes and effects of each failure mode are included in Table 3.

During the taxonomy formulation process, we sought failure modes that could be described in terms of the elemental physics of the failure. Each new term added to the taxonomy had to be mutually exclusive with existing terms such that coverage was provided to an area not already covered in the taxonomy. If the term was not mutually exclusive but instead overlapped to some degree with an existing term, then the following categorization algorithm was employed:

1) The new term might be a superset of the existing term it overlaps with, in which case the new term might be used as a primary identifier.

2) The new term might be similar enough to an existing term that it might be categorized as a comparable term (synonym) rather than entering it into the basis as a new item.

3) The new term and the term which it overlaps may need to be combined or replaced by a slightly broader term.

4) The new term and/or the term which it overlaps may need to be replaced by a more specific term that provides mutual exclusivity.

3.3 Comparing Taxonomy with NASA Spacecraft Data

3.3.1 Investigating NASA's Failure Reports.

During the summer of 2003, one of NASA's problem report databases was investigated to compare our theoretical failures with reported failures. The problem report database contains development and operations anomalies and failure data for more than 300 missions [8]. The primary purpose of the database is to log any problems discovered during spacecraft development and testing to ensure proper corrective action is taken.

Due to the substantial number of reports in the problem reporting system and the predefined number of days we were allowed to access the database, we chose to concentrate our data mining efforts on a single spacecraft, referred to here as Spacecraft A. The search for problem reports was further limited to those failures for Spacecraft A that were encountered during ground testing (i.e., before the spacecraft had been launched), because the opportunity for destructive physical analysis (DPA) was available to determine the root cause of the problem if DPA was deemed necessary. The database contained 2750 ground test problem reports for Spacecraft A divided into the categories shown in Table 4.

Table 4. Problem reports per category for Spacecraft A.

Problem Report Category	**Percentage of Failures**
Software	33.9
Testing equipment and Testing procedure faults	24.7
Other (Miscellaneous, Not a problem, Damage from mishandling)	20.7
Design	11.9
Manufacture, Workmanship and Adjustment	7.6
Part failure	1.2
TOTAL	**100.0**

More than one-third, 933 out of 2750, of the problems encountered while performing ground tests for Spacecraft A were software related. The number of part failures was identified as 1.2 percent of the overall failures, which corresponds to 33 out of 2750 problems/failures. The percentage of software failures (i.e., "bugs") indicates the extent to which software was utilized in Spacecraft A. Problems due to incorrect software could theoretically result in mission failure. However, software can be updated after launch assuming the spacecraft telecommunications equipment hasn't encountered a failure, whereas a failed component cannot be replaced once the spacecraft has launched. Although some systems incorporate redundancy, efforts toward the reduction of part failure in spacecraft subsystems are still worthwhile endeavors.

3.3.2 Retrieving Failure Modes from Problem Reports.

We reviewed all of the problem reports for Spacecraft A that were categorized as design, manufacturing or part failures. Some of the failures we encountered include: an improperly bonded capacitor that led to an open circuit; electrostatic discharge occurred 5 times; undercurrent; factory escape (internally shorted capacitor); undetermined (component destroyed during DPA); coronal discharge occurred 5 times; traces on a backplane were too thin; electrical overstress, manufacturing defects that include poor bonding (which occurred multiple times) and thermal fatigue due to coefficient of thermal expansion mismatch. The primary effects of these failures were often open or short circuits, while the secondary effects (e.g., an incorrect voltage reading or a device not operating as expected) usually provided the indication of failure. Because the resolution of failures to their root cause is secondary in importance to properly resolving each failure, many problem reports did not contain the detailed information we needed to accurately assign a failure mode.

3.3.3 Updating Taxonomy.

Prior to reviewing the problem reports, coronal discharge, arc discharge, glow discharge, undercurrent and overcurrent were not included in our taxonomy. Literature review of coronal discharge led us to arc discharge and glow discharge. Likewise, the prospect of undercurrent as a failure mode exposed overcurrent as a similar failure mode.

4. RESULTS: ELECTRICAL FAILURE MODE DEFINITIONS

The electrical failure mode taxonomy presented here supplements prior work by Roberts, Tumer et al. and Tumer, Stone et al. [8, 11], which details a mechanical failure mode taxonomy for use as a failure identification tool during conceptual design. The electrical failure mode taxonomy includes a variety of failure modes that occur during manufacturing and/or during use and are exhibited by integrated circuits (ICs) and/or discrete components. Based on the breadth of the resources used to develop the list, the taxonomy presented here contains an estimated 75% of existing physics-based electrical failure modes.

After deriving the list of electrical failure modes, the failure modes were organized into high-level categories based on failure mode similarity. The use of a primary identifier to categorize the failure modes maintains consistency with the previously existing mechanical failure mode taxonomy and adds structure and organization to the list of failure modes. In the following sections, brief definitions of the electrical failure modes are presented alphabetically by primary identifier in the same order they are shown in the electrical failure mode taxonomy in Tables 2 and 3. Note that typical causes and effects are identified in the definition of each of the following failure modes.

4.1 Failure Modes Identified as a Bonding Defect

Bond pad contamination [19] is caused by wafer processing, plastic package outgassing or epoxy die attach outgassing, and bleedout. Contaminants accelerate failure by reducing the onset temperature or the time to failure due to intermetallic growth. Bond pad contamination can lead to bond resistance change. Contaminants in the wire itself and those introduced from leadframe plating accelerate breakage of the wire, leading to open circuits.

Bond pad cratering [19] is the result of microcracks formed in the silicon and oxide layers under the bond pads due to stresses introduced during the dynamic force of the gold ball at touch-down impact, the static force applied after touch-down, ultrasonic energy, mechanical vibrations before or after bonding, and the hardness of the gold ball. The effect of cratering is a reduction in the strength of the silicon oxide layers under the bond pads.

Bond resistance change [19] is essentially a poor contact at the bond surface that is caused by intermetallic growth, Kirkendall voiding, bond pad contamination, corrosion, intermetallic formation, and manufacturing errors. A bond is considered failed open when its resistance is increased by 20 milliohm from its original value.

Bondline thickness error [19] is caused by a lack of control in die alignment or the latent evaporation of die adhesive solvent that leads to either too much or too little die adhesive material. When the bondline thickness approaches the dimensions of the filler, reduced bonding strengths can result. Very thin bondlines can lead to an increased stress on the die and an increase in the volume resistivity. For materials containing a solvent, the latent evaporation of solvent will change the viscosity and affect bondline thickness. The stress decreases or increases with the elastic modulus of the die bonding material.

Incorrect bond placement [19] is attributed to poor process controls. The result of incorrectly placed bonds is short circuits or crossed wires. Ball bonds that are inaccurately located can touch metallization lines, leading to incorrect signal paths.

Irregular bump size [19] is caused by contamination, plating defects, or insufficient bonding pressure in tape automate bonding. The effect of irregular bump size is an inadequate bond between the metallized tape and some of the bumps.

Poor bonding [2, 20] is caused by incorrect bonding parameters, poor surface cleaning before bonding, excessive bonding force, or excessive bonding temperature. Poor bonding results in an open circuit, but in the case of an excessively high bonding force, poor bonding can lead to a short between the pad and substrate. Poor bonding has also been referred to as poor adhesion.

Poor die-attach [19, 20] occurs when the high surface energy of the Si forms an oxide layer that doesn't allow the silicon to form a eutectic bond. Poor die-attach can result in poor and non-uniform thermal conductivity causing circuit performance degradation and ultimately short or open circuits.

4.2 Failure Modes Identified as a Form of Breakdown

Arc discharge [21] is characterized by low voltage and large current. As the voltage between two contacts is increased, the resulting electric field between the contacts accelerates free electrons, causing them to strike neutral gas molecules. If the free electrons have sufficient kinetic energy imparted by the electric field, they strike the gas molecules, creating additional free electrons as electron-ion pairs. This produces a multiplicative production of free electrons and positive ions. The number of free electrons increases as an avalanche effect. The breakdown voltage is dependent on the gas, contact separation and pressure. The arcing results in a short. The arc extinguishes when the contact separation increases (e.g., in the case of a switch) or when the current magnitude is decreased below the minimum arcing current.

Coronal discharge [22] is similar to an arc discharge in terms of the physics of failure but is characterized by an electric field in the presence of a vacuum or critical pressure region. Similar to ESD, coronal discharge results in a large magnitude short duration discharge current that can lead to a loss of data, dielectric breakdown, junction short circuits, and cracks (open circuits) between isolated regions.

Electrostatic discharge (ESD) [2, 20, 21] is characterized by a separation and buildup of static charge that occurs when dissimilar materials are rubbed together in a low humidity environment. Such a charge buildup creates intense electric fields and a significant voltage difference (ranging from 100 V to 20 kV). ESD occurs through either direct conduction or the breakdown of the intervening air that is visible as intense arc. ESD results in a large magnitude, short duration discharge current. These large currents are sufficient to cause dielectric breakdown, junction short circuits and cracks (open circuits) between isolated regions. ESD can also cause bridges (shorts) between two metal conductors. Damage from ESD could be immediate as well as latent.

Gate oxide breakdown [20, 23] is caused by defects in the gate oxide (such as pinholes or thin spots) or a high voltage across the gate oxide (such as ESD or EOS) that results in an excessive electric field. The excessive electric field causes Si and SiO2 to melt producing Si filaments that short the polysilicon gate to the Si surface. The resulting gate oxide shorts may include shorted GD (gate-drain) or shorted GS (gate-source). The effect of the short is current leakage. Failure depends on the seriousness of the defect and the voltage experienced at the defect site.

Glow discharge [21] is characterized by large voltage and small current. As the voltage between two contacts is increased, the resulting electric field between the contacts accelerates free electrons, causing them to strike neutral gas molecules. If the free electrons have sufficient kinetic energy imparted by the electric field, they strike the gas molecules, creating additional free electrons as electron-ion pairs. This produces a multiplicative production of free electrons and positive ions. The number of free electrons increases as an avalanche effect. A region near the cathode develops a faint glow. As the current density increases, the cathode begins heating. The quick heating causes vaporization of the contact metal, which may result in a rapid drop in contact voltage marking the beginning of an arc discharge.

Time dependent dielectric breakdown (TDDB) [2, 23] is caused by poor processing, particulate defects or contaminants in the thin oxide mask, stacking faults in the oxides, or by imperfections in the SiO2 that result in thinning of the dielectric. The resulting shorts may occur during wafer fabrication or may be latent.

4.3 Failure Modes Identified as Contamination

Ionic contamination [2, 19, 20] occurs when mobile ions (mainly Na+) are introduced into semiconductor devices. In general, such contamination is caused by ionic impurities present in the die attach adhesives (such as aqueous extractable chloride and sodium), environment, human contact, processing materials, and packaging. Ionic contamination affects the charge distribution in the transistor channel region. Contamination in hermetic cases is the result of soldering residues, photolithography residues, and etching residues. Contaminants in non-hermetic cases can be introduced from the molding compound and any die coating or die-attach coating enclosed by the encapsulant. Impurities normally exist in both epoxy resin and in fillers. The presence of mobile ions at the SiO2 interface along the transistor channel causes the threshold voltage to change. The spreading of ionic contamination can lead to conduction (shorts) between adjacent devices outside the active region of a transistor, threshold voltage shift, direct chemical attack (corrosion), current leakage near junctions, and degradation of bonds. Contamination in hermetic and non-hermetic packages can lead to leakage current and corrosion that eventually results in open circuits. The magnitude of the leakage current and the time to failure is strongly dependent on the amount of ionic impurities present.

Bridging occurs when a piece of conducting contaminant or debris forms an undesired bridge between nodes resulting in a short circuit. An example of bridging could be a piece of aluminum threading from the drilling and tapping process falling and becoming lodged between the 12 V and reference pins of a component on a printed circuit board.

4.4 Failure Mode Identified as Cracking

Cracking [19] can occur in many forms. For non-hermetic packages, the failure mode is largely a function of package-induced surface shear stresses. Cracks in non-hermetic packages can be caused by a large difference in CTE between the encapsulant, leadframe, and die; the pressure during reflow due to the vaporizing moisture absorbed by the package; or moisture ingress that collects at the delaminated surfaces. For tape automated bonding, cracking results from the concentration of stress on the passivation layer under the TAB bump during bonding; the failure may occur during thermal cycling. The concentration can be the result of misaligned leads or excessive bonding force. Vertical die attach cracking can be attributed to locally higher stresses caused by a coefficient of thermal expansion mismatch between the chip and package, while horizontal die attach cracking is due to the saw-and-break method of die separation. For the hermetic case package, cracking in copper and Alloy 42 leadframe packages can be caused by thermal stresses while cooling. Cracks in ceramic packages can be thermally induced by CTE mismatch during thermal cycling by very low levels of thermal stress or by wave soldering of through hole components. In the case of leads, bending of leads can result in transgranular cracks and the propagation of cracks in the lead. Cracks can provide sites for moisture ingress, which can lead to the formation of additional cracks that finally result in corrosion and shorts. Cracks can also lead to die fracture during temperature cycling or a loss of adhesion between the molding compound and the chip. Cracks in conductors severely reduce the durability of the leads by reducing strength and introducing stress concentration areas. As the maximum stress occurs near the intersection between the solder joint and the beam lead, fatigue cracking of the lead can initiate and propagate through the thickness of the lead.

4.5 Failure Modes Identified as a Form of Diffusion

Electromigration [2, 20, 24, 25] is a form of metallization failure that is caused by poor design, processing mask defects that result in missing conducting material on the wire, small spacings between metal conductors on PCBs, processing residues, exposure to humid and/or polluted environments, and scratches. Electromigration is the resulting motion of the atoms of a conductor when an electric current passes through a conductor that has missing conducting material. Thermally activated ions of the conductor, which normally self diffuse in all directions, are given a direction of net motion due to momentum transfer from the conducting electrons. The ions move "downstream" with the electrons. Positive divergence of the ions can lead to an accumulation of vacancies that form a void in the metal (causing resistance increase) and ultimately an open circuit, while a negative divergence of the ions can lead to a buildup of metal, called hillock, which cause a short circuit to adjacent or overlying metal. Electromigration is most serious in metal wires where the current density is excessively high.

Galvanic corrosion [15, 20] is a form of metallization failure that occurs when two dissimilar metals are in the presence of moisture, DC operating potentials, and ions (mainly Cl- or Na+). The ions act as a catalyst. The potential difference between the dissimilar metals produces a current flow through the connecting electrolyte leading to corrosion of the more anodic metal. The result of corrosion is a decrease in strength of the conductor that eventually leads to mechanical failure and an open circuit in the metallization. Failure rates due to corrosion are influenced by the humidity and temperature.

Interdiffusion [14, 19] can occur when dissimilar bulk materials are in intimate contact at a surface. Molecules from one material can migrate into the other and vice-versa via diffusion. Interdiffusion in the form of intermetallic formation in wire bonding occurs between dissimilar metals and is dependent on bond time and temperature. During the solder joint reflow process, interdiffusion may occur in three forms that include dissolution of the base metals into the solder, intermetallic formation at the interface, and precipitation of intermetallics in solder joints. If the effective diffusion rates between the materials are unequal, one of the materials may suffer a depletion of atoms leading to Kirkendall voiding. Interdiffusion, which provides interfacial adhesion, can lead to stress cracking or brittle bonds that can break either under vibration or flexing due to metal fatigue. Excessive amounts of intermetallic compound and the package being exposed to high temperatures (400-450 C) forms Kirkendall voids at the bond interface. These voids can coalesce causing bond strength degradation, lifting, increased joint electrical resistance, or open circuits. A common example in electronic packages is the leaching of gold into aluminum in wire bonds leading to purple plague.

Interfacial de-adhesion [14] occurs at the interface between two adhering materials. Work is required to create an adhesive failure at the interface. The interfacial adhesive strength between two dissimilar materials, which depends on the chemical and mechanical properties of the interface, can be enhanced by interdiffusion. Interfacial bonding strength between pairs of materials is characterized in terms of the electron binding energy between those materials. Examples of interfacial de-adhesion are delaminations in laminated composite materials and adhesion failures in bonded joints. Interfacial de-adhesion in electronic packages are failures at interfaces of a die and the attach material or at the interface of a wire bond and the bond pad.

Silicon interdiffusion [20, 24] is a form of electromigration leading to contact leakage as silicon migrates out of the contact allowing aluminum to diffuse into the resulting void to form a short to the substrate.

4.6 Failure Mode Identified as a Form of Fatigue

Thermal fatigue [2] is a result of CTE (coefficient of thermal expansion) mismatch or poor bonding. In terms of electrical systems, the result of thermal fatigue is ultimately an open circuit.

4.7 Failure Modes Identified as Hot Carrier Induced Degradation

Charge trapping [20] is caused by poor designs, imperfect fabrication processes or spot defects that cause transistors to have inadequate channel lengths or inadequate gate oxide thicknesses. These defects can allow some carriers to gain enough energy in the transistor channel to inject into the gate oxide and become trapped. Once the charge is trapped, the charge distribution along the transistor channel is changed and transistor characteristics altered leading to decreased transconductance, increased substrate current, or increased threshold voltage. This failure affects the charge distribution in the transistor channel region.

Interface trap generation [20] is attributed to poor designs, imperfect fabrication processes or spot defects that cause transistors to have inadequate channel lengths or inadequate gate oxide thicknesses. These defects can allow high-energy carriers moving along the channel to create electron-hole pairs by collisions near the drain, generating oxide interface traps. The charge distribution along the transistor channel is changed and transistor characteristics altered leading to decreased transconductance, increased substrate current, or increased threshold voltage. This failure affects the charge distribution in the transistor channel region.

4.8 Failure Mode Identified as Latch-up

Latch-up [20] is caused by the improper design or manufacture that leads to the substrate, the n- or p-well, or the diffusion regions being cross-connected with common base-collector junctions in a CMOS structure on silicon. The interconnection may lead to saturation and the power supply being connected across a low resistance path to ground.

4.9 Failure Mode Identified as Mask Defects

Mask defects [20] are regions with extra or missing material in one of the conductive, semiconductive, or insulating layers. The effects of mask defects are open circuits, short circuits, and transistor stuck-on (i.e. shorted drain-source). Processing mask defects are also referred to as spot defects.

4.10 Failure Modes Identified as a Form of Noise

Alpha particle induced soft errors [17, 20, 24] occur when a sufficient number of the minority carriers generated by an alpha particle or a cosmic ray are collected on a storage node to pull the node from logic high to logic low thereby destroying the memory state. Alpha particles can be produced by cosmic rays or the radioactive decay of uranium and thorium impurities incorporated in IC packaging materials. The error is “soft” because the memory state becomes correct again when a new value is stored.

Common impedance coupling [21, 26] is a design problem that can occur when at least three conductors are present with one conductor serving as a common reference. Coupling arises when the common impedance voltage drops (i.e., the voltage drops across the common return) are significant with respect to the voltage levels of the circuit. Common impedance coupling is a near-field intrasystem (i.e. the circuit interferes with itself) coupling problem that occurs at low frequencies (i.e., frequencies below the GHz range) that leads to functional problems within the circuit.

Electric field coupling is a form of electromagnetic interference characterized by a high voltage in close proximity to the receptor that creates an electric field of sufficient magnitude to result in interference in a receptor. Interference occurs if the received energy is of sufficient magnitude and/or spectral content at the receptor input to cause the receptor to behave in an undesired fashion. Electric field coupling can lead to false internal chip signals and other functional problems within the circuit. Capacitive crosstalk is a form of electric field coupling.

Electromagnetic pulse (EMP) [21] is caused by the intense electromagnetic wave created by the charge separation and movement within a nuclear detonation. Semiconductor devices within range of the electromagnetic wave are destroyed.

Electromagnetic radiation [21] is a form of electromagnetic interference characterized by high frequency waves and a relatively large distance of separation between the source and the receptor. Electromagnetic radiation is the unintentional transmission or reception of electromagnetic energy that results in undesired behavior of the receptor. The unintentional transfer of energy causes interference only if the received energy is of sufficient magnitude and/or spectral content at the receptor input to result in false internal chip signals or other undesired behavior in the receptor circuit.

Ground bounce [26] refers to shifting of the internal ground reference voltage. Lumped ground pins and fast output transition times as well as a poor ground connection increase the likelihood of ground bounce within the logic package. Ground bounce voltages are proportional to the rate of change in current through the ground pin. Ground bounce interferes with signal reception and can lead to double clocking.

Magnetic field coupling is a form of electromagnetic interference characterized by large currents that produce magnetic fields and interfere with the receptor. Interference occurs if the received energy is of sufficient magnitude and/or spectral content at the receptor input to cause the receptor to behave in an undesired fashion. Magnetic field coupling can lead to false internal chip signals and other functional problems within the circuit.

4.11 Failure Modes Identified as a Form of Overstress or Incorrect Current Magnitude

Electrical overstress (EOS) [20] is caused by improper application or handling of an integrated circuit. Electrical transients induced from electromagnetic radiation (i.e., nuclear radiation, electromagnetic pulses, radar, lightning, or switched transients) cause a higher than specified current at some semiconductor junctions that generates additional heat and could ultimately melt the junctions causing open circuits or short circuits. Damage from EOS could be immediate as well as latent.

Overcurrent refers to large currents that may be caused by overloading or short circuits. Overcurrent causes a severe heat buildup that results in thermal breakdown, vaporization of the conductor (i.e. an open circuit), and/or a fire induced by overheating materials surrounding the conductor.

Undercurrent indicates an insufficient current magnitude that may result from a conducting medium at an excessively low temperature (which decreases electron velocity) or a discharged power source. The effects of undercurrent include reduced device response times or an inoperative component/device/system.

4.12 Failure Mode Identified as Punch-through

Punch-through [20, 23] occurs when the channel length is so small that depletion regions for the source and drain interact to reduce the barrier for electron flow between these two regions. Manufacturing defects and poor design can lead to a short channel length. Punch-through causes a shorted DS (drain-source) regardless of the voltage at the gate. As the device feature size decreases, short channel effects in MOS transistors become significant.

4.13 Failure Mode Identified as Voiding

Voiding [19] in the die attach is caused by the oxidation of bonding surfaces. For a non-hermetic case, voids in the gel can form when the rate of change of temperature is faster than the permeation rate of the water in the gel. Voids in the die attach can lead to junction temperature increases and die attach cracking during temperature cycling. Void formation in a non-hermetic case can lead to corrosion.

5. CONCLUSIONS AND FUTURE WORK

To make use of the Function-Failure Design method, which links function to potential failure(s) during conceptual design, a comprehensive failure mode taxonomy is needed. In its prior state, this taxonomy was limited to an extensive list of mechanical failure modes. We define failure in general as the combination of the cause of the failure mode, the failure mode, and the effect of the failure mode that renders an electrical, mechanical or electromechanical device incapable of satisfactorily performing its intended function under normal usage conditions. Literature review, personal experiences, expert elicitation, and our definition of failure mode were combined to ascertain the causes, failure modes, and effects that describe the manners in which electrical components fail. We summarize this work in the form of an electrical failure mode taxonomy containing 38 electrical failure modes organized into 13 categories. Because these failure modes are at the physics of failure level, they are appropriate for design at the component or subsystem level. The contribution of this work is a set of failure analysis definitions and a taxonomy of electrical failure modes.

Future work is twofold. First, we would like to extend the taxonomy to include any additional electrical failure modes, composite and polymer failure modes, and possibly software failure modes. Second, we would like to adapt the FFD method and the failure cause/effect relationship in an effort to design conceptually at the system level. Currently, we have a FFD database (containing function, component, and failure information) and functional models (at different levels of detail) for two major spacecraft subsystems that we will use in the near future to test the FFD method as a tool that can be utilized during the conceptual stages of spacecraft subsystem (electrical and mechanical) design.

ACKNOWLEDGMENTS

We would like to thank Arthur Brown for demonstrating how to navigate NASA's problem report database.

This work is supported by the NASA Ames Research Center under grant NCC 2-5423. Any opinions or findings of this work are the responsibility of the authors and do not necessarily reflect the views of the sponsors or collaborators.

REFERENCES

1. Pecht, M. and Ramappan, V., 1992, "Are Components Still the Major Problem: A Review of Electronic System and Device Field Failure Returns," IEEE Transactions on Components, Hybrids, and Manufacturing Technology, **15** (6): 1160-1164.
2. Fantini, F. and Morandi, C., 1985, "Failure Modes and Mechanisms for VLSI ICs - A Review," Electronic Circuits and Systems, **132** (June): 74-81.
3. Tumer, I. Y. and Stone, R. B., 2001, "Analytical Methods for Mapping Function to Failure During High-Risk Component Development," Design Engineering Technical Conferences, Pittsburgh, PA U.S.A.
4. Carter, A. D. S., 1997, *Mechanical Reliability and Design*, John Wiley & Sons.
5. Price, C. P., 1996, "Effortless Incremental Design FMEA," Annual Reliability and Maintainability Symposium, Las Vegas, NV U.S.A.
6. Hunt, J. E., Pugh, D. R. and Price, C. P., 1995, "Failure Mode Effects Analysis: A Practical Application of Functional Modeling," Applied Artificial Intelligence, **9** (1): 33-44.
7. Wirth, R., Berthold, B., Kramer, A. and Peter, G., 1996, "Knowledge-based Support Analysis for the Analysis of Failure Modes and Effects," Engineering Applications of Artificial Intelligence, **9** (3): 219-229.
8. Roberts, R. A., Tumer, I. Y., Stone, R. B. and Brown, A. F., 2003, "A Function-based Exploration of JPL's Problem/Failure Reporting Database," International Mechanical Engineering Congress and Expo, Washington, D.C. U.S.A.
9. Arunajadai, S. G., Stone, R. B. and Tumer, I. Y., 2002, "A Framework For Creating a Function-Based Design Tool for Failure Mode Identification," ASME Design Engineering Technical Conference, Design Theory and Methodology Conference, Montreal, Canada.
10. Hirtz, J., Stone, R., McAdams, D., Szykman, S. and Wood, K., 2002, "A Functional Basis for Engineering Design: Reconciling and Evolving Previous Efforts," Research in Engineering Design, **13** (2): 65-82.
11. Tumer, I. Y., Stone, R. B. and Bell, D. G., 2003, "Requirements for a Failure Mode Taxonomy for Use in Conceptual Design," International Conference on Engineering Design, Stockholm Sweden.
12. Bohm, M., March 2004, Design Engineering Lab: Design Repository Login, http://module.basiceng.umr.edu:8080/view/.
13. Bohm, M., Stone, R. and Szykman, S., 2003, "Enhancing Virtual Product Representations for Advanced Design Repository Systems," Proceedings of DETC2003, Chicago, IL, DETC2003/CIE-48239.
14. Dasgupta, A. and Pecht, M., 1991, "Material Failure Mechanisms and Damage Models," IEEE Transactions on Reliability, **40** (5): 531-536.
15. Collins, J. A., 1993, *Failure of Materials in Mechanical Design*, John Wiley & Sons, New York, NY U.S.A.
16. Collins, J. A., Hagan, B. T. and Bratt, H. M., 1976, "The Failure-Experience Matrix: A Useful Design Tool," Journal of Engineering for Industry, **98** (3): 1074-1079.
17. Evans, J., Lall, P. and Bauernschub, R., 1995, "A Framework for Reliability Modeling of Electronics," Reliability and Maintainability Symposium, Washington, DC U.S.A., 144-151.
18. Stamatis, D. H., 1995, *Failure Mode and Effect Analysis, FMEA from Theory to Execution*, Milwaukee, WI, ASQ Quality Press.
19. Bauernschub, R. and Lall, P., 1994, "A PoF Approach to Addressing Defect-related Reliability," Electronics Manufacturing Technology Symposium, La Jolla, CA U.S.A., 38-49.
20. Hao, H., 1993, *Electrical Failure Modes in CMOS Logic Integrated Circuits*, Chapter 2: Overview of Failure Mechanisms and Failure Modes in CMOS ICs, Stanford University, Stanford, CA USA.
21. Paul, C. R., 1992, *Introduction to Electromagnetic Compatibility*, John Wiley & Sons, Inc., New York.
22. Oberhettinger, D. and Whittlesey, A., January 25, 2004, Protect Against Corona Discharge and High Voltage Breakdown (1960's-Present), PLLS Database Entry: 0598, http://llis.nasa.gov/llis/plls/index.html.
23. Soden, J. M. and Hawkins, C. F., 1989, "Electrical Properties and Detection Methods for CMOS IC Defects," European Test Conference, Paris France.

24. Woods, M. H., 1986, "MOS VLSI Reliability and Yield Trends," Proceedings of the IEEE, **74** (12): 1715-1729.
25. Vaughen, B. K., Roth, J. A., Steppan, J. J., Hall, L. C. and Major, C. P., 1988, "Electrolytic Copper Migration in Accelerated Tests," Journal of the Electrochemical Society, **135** (8): 2027-2033.
26. Johnson, H. W., 1993, *High Speed Digital Design: A Handbook of Black Magic*, Prentice-Hall, Inc., Upper Saddle River.

Table 1. Mechanical failure mode taxonomy.

Primary Identifier	Failure Mode	Definition
Buckling (High and/or point load geometric configuration)	Buckling	An increased deflection of a member after a slight change in load as a result of the geometrical configuration and the combination of magnitude and/or point of load.
Corrosion (Material deterioration due to chemical or electrochemical interaction with environment)	Biological corrosion	The corrosive process resulting from the food ingestion and waste elimination by microorganisms or macro organisms. The waste products of these living organisms act as corrosive media.
	Cavitation erosion	A form of chemical corrosion caused by differences in vapor pressure. Bubbles and cavities within a fluid collapse adjacent to the pressure vessel walls and cause particles of the surface to be expelled thereby baring the material below the surface to the corrosive medium.
	Corrosion fatigue	A failure mode in which corrosion and fatigue combine with each process accelerating the other. The corrosive process forms pits and surface discontinuities that act as stress raisers and accelerate fatigue failure. Cyclic loads or strains lead to cracking and flaking of the corrosion layer baring the material below the surface to the corrosive medium.
	Crevice corrosion	A form of corrosion that occurs within crevices, cracks or joints. Small volume regions of stagnant solution are trapped in contact with the corroding metal.
	Direct chemical attack	A common form of corrosion that occurs when the surface of the machine part exposed to the corrosive media is attacked more or less uniformly over its entire surface. The result is a progressive deterioration and dimensional reduction of load-carrying net cross section.
	Erosion corrosion	A form of chemical attack that occurs when abrasive or viscid material continuously flows past a surface thereby baring the material below the surface to the corrosive medium.
	Galvanic corrosion	Electrochemical corrosion of two dissimilar metals in electrical contact. Current flows through a connecting pool of electrolyte or corrosive medium and leads to corrosion.
	Hydrogen damage	Any damage to a metal caused by the presence of hydrogen or the interaction with hydrogen. Such damage includes hydrogen blistering, hydrogen embrittlement, hydrogen attack, and decarburization.
	Intergranular corrosion	A form of attack that occurs when the formation of galvanic cells precipitate corrosion at grain boundaries of copper, chromium, nickel, aluminum, magnesium, and zinc alloys due to the alloy being improperly heat treated or welded.
	Pitting corrosion	A form of corrosion similar to crevice corrosion leading to the localized development of array of holes or pits that penetrate the metal. The pit can be initiated by a small surface scratch, a defect, or a momentary attack due to a random variation in fluid concentration.
	Selective leaching	A form of corrosion in which one element is preferentially removed from an alloy to obtain a metal that is more resistant to the intended environment.
	Stress corrosion	Occurs when the applied stresses on a machine part in a corrosive media generate a field of localized surface cracks, which usually occur along grain boundaries.

Table 1 continued. Mechanical failure mode taxonomy.

Primary Identifier	Failure Mode	Definition
Creep (Plastic deformation)	Creep	Occurs when the plastic deformation in a machine member accrues over a period of time under the influence of stress and temperature. The accumulated dimensional changes eventually interfere with the ability of the machine part to satisfactorily perform its intended function
	Creep buckling	A delayed result of creep whereby an unstable combination of the loading and geometry of a machine part exceed the critical buckling limit.
	Stress rupture	Rupture into two pieces as a result of stress, time, and temperature. The steady-state creep growth period is often short or nonexistent.
	Thermal/stress relaxation	The relaxation of a prestrained or prestressed member due to the dimensional changes resulting from the creep process.
Ductile deformation (Ductile material)	Brinelling	A static force induced permanent surface discontinuity of significant size occurring between two curved surfaces in contact as a result of local yielding of one or both mating members.
	Force induced elastic deformation	Occurs when the imposed operational loads or temperatures in a machine member result in elastic (recoverable) deformation such that the machine can no longer satisfactorily perform its intended function.
	Yielding	Occurs when the imposed operational loads or motions in a ductile machine member result in plastic (unrecoverable) deformation such that the machine can no longer satisfactorily perform its intended function.
Fatigue (Fluctuating loads or deformation)	High cycle fatigue	The sudden separation of a machine part into two or more pieces occurring when loads or deformations are of such magnitude that more than 10,000 cycles are required to produce failure.
	Impact fatigue	Failure of a machine member by the nucleation and propagation of a fatigue crack that occurs as a result of repetitive impact loading.
	Low cycle fatigue	The sudden separation of a machine part into two or more pieces occurring when loads or deformations are of such magnitude that less than 10,000 cycles are required to produce failure.
	Surface fatigue	Pitting, cracking, and spalling of contacting surfaces (often rolling surfaces) that occur as a result of cyclic contact stresses and cyclic shear stresses below the contacting surface. The cyclic subsurface shear stresses generate cracks that propagate to the contacting surface and dislodge particles to produce surface pitting.
	Thermal fatigue	Occurs when fluctuating temperature fields in the machine part cause load or strain cycling to the point of failure of the machine part.
Fretting (Small amplitude fluctuating loads or deformations at joints not intended to move)	Fretting corrosion	Surface degradation of the material from which the part is made that occurs as a result of fretting action.
	Fretting fatigue	The premature fatigue fracture of a machine part that occurs as a result of conditions that simultaneously produce fretting action and fluctuating loads or strains.
	Fretting wear	The presence of fretting action causes a change in the dimensions of mating parts. The changes in dimensions become large enough to interfere with proper design function or large enough to produce geometrical stress concentrations of such magnitude that failure ensues as a result of excessive local stress levels.
Galling & Seizure (Sliding surfaces)	Galling	Massive surface destruction by welding and tearing, plowing, gouging, significant plastic deformation of surface asperities, and metal transfer between the two surfaces. Occurs when two sliding surfaces are subjected to such a combination of loads, sliding velocities, temperatures, environments, and lubricants that significant impairment to intended sliding surfaces results.
	Seizure	An extension of the galling process that occurs when the two parts are become welded together so that relative motion is no longer possible.

Table 1 continued. Mechanical failure mode taxonomy.

Primary Identifier	Failure Mode	Definition
Impact (Impact load of large magnitude)	Impact deformation	The intolerable elastic or plastic deformation that occurs as a result of impact and causes failure.
	Impact fracture	The magnitudes of the stresses and strains that occur as a result of impact are high enough to cause separation into two or more parts.
	Impact fretting	The fretting action induced by small lateral relative displacements between two surfaces that are not intended to move as they impact together. The small displacements are caused by Poisssan strains or small tangential "glancing" velocity components.
Radiation (Nuclear radiation)	Radiation damage	When the exposure to a nuclear radiation field result in changes in material properties such that the machine part is no longer able to perform its intended function. Radiation exposure usually triggers some other failure mode and is often related to a loss in ductility.
Rupture (Separate into two or more parts)	Brittle fracture	Primary interatomic bonds being broken as a result of elastic deformation and the member, which exhibits brittle behavior, separates into two or more pieces. The fracture exhibits a granular, multifaceted surface.
	Ductile rupture	The plastic deformation in a machine part, which exhibits ductile behavior, to the point of the member separating into two pieces. A dull, fibrous fracture surface results from the propagation of internal voids.
Spalling (Particle spontaneously dislodged from surface)	Spalling	A particle being spontaneously dislodged from the surface of a machine part and prevents the proper function of the member.
Wear (Undesired change in dimension)	Abrasive wear	Occurs when wear particles are removed from the surface by plowing, gouging and cutting action of the asperities of a harder mating surface or by hard particles trapped between the mating surfaces.
	Adhesive wear	A type of wear caused by high local pressure and welding at asperity contact sites followed by motion-induced plastic deformation and rupture of asperity junctions. The result of this form of wear is metal removal or metal transfer.
	Corrosive wear	Occurs when adhesive wear or abrasive wear are combined with conditions that lead to corrosion.
	Deformation wear	A form of wear caused by repeated plastic deformation at the wearing surfaces. A matrix of cracks are produced that grow and coalesce to form wear particles.
	Impact wear	A form of wear caused by repeated elastic deformation at the wearing surface.
	Surface fatigue wear	An occurrence of wear associated with curved surfaces in rolling or sliding contact. Subsurface cyclic shear stresses produce microcracks that propagate to the surface and cause macroscopic particles to be removed by spalling thereby forming wear pits.

Table 2. Electrical failure mode taxonomy.

Primary Identifier	Failure Mode	Definition
Bonding defect	Bond pad contamination	Impurities in the bonding pad.
	Bond pad cratering	Microcracks in the silicon and oxide layers under the bond pads.
	Bond resistance change	Poor contact at the bond surface that results in bond resistance change; bonds are considered failed open when its resistance is increased by 20 milliohm from its original value.
	Bondline thickness error	Too much or too little die adhesive material.
	Incorrect bond placement	Incorrectly located bond.
	Irregular bump size	Contamination, plating defects, or insufficient bonding pressure in tape automate bonding leading to inadequate bonding between the metallized tape and some of the bumps.
	Poor bonding	Incorrect bonding parameters, poor surface cleaning before bonding, excessive bonding force or excessive bonding temperature.
	Poor die-attach	Non-eutectic bonded silicon.
Breakdown	Arc discharge	Voltage between two contacts increases to the point of breaking down the gas between contacts.
	Coronal discharge	An electric field in the presence of a vacuum or critical pressure region leading to a voltage discharge through the low pressure medium.
	Electrostatic discharge (ESD)	Static charge separation leading to high voltages ranging from 100 V to 20 kV being quickly discharged.
	Gate oxide breakdown	An excessive electric field across the gate oxide causing Si and SiO2 to melt producing Si filaments that short the polysilicon gate to the Si surface.
	Glow discharge	The voltage between two contacts being sufficient to cause the region near the cathode to heat and glow; such heating causes vaporization of the contact metal and may result in a rapid drop in contact voltage marking the beginning of an arc discharge.
	Time dependent dielectric breakdown (TDDB)	Latent shorts resulting from particulate defects, contaminants in the thin oxide mask, or imperfections in the SiO2.
Contamination	Bridging	Occurs when a piece of conducting contaminant or debris forms an undesired bridge between nodes and results in a short circuit.
	Ionic contamination	The presence of mobile ions (mainly Na+) in semiconductor devices.
Cracking	Cracking	The manifestation of a flaw, defect, or weak spot in the form of narrow break.
Diffusion	Electromigration	The resulting motion of the atoms of a conductor when an electric current passes through a conductor having missing conducting material; thermally activated ions of the conductor, which normally self diffuse in all directions, are given a direction of net motion due to momentum transfer from the conducting electrons causing the ions move "downstream" with the electrons.
	Galvanic corrosion	Occurs when two dissimilar metals are in the presence of moisture, DC operating potentials, and ions. A connecting pool of electrolyte or corrosive medium completes the circuit between the two metals. The ensuing current leads to corrosion.
	Interdiffusion	Two different bulk materials in intimate contact at a surface whereby molecules of one material to migrate into the other by diffusion and vice-versa.
	Interfacial de-adhesion	A delamination or adhesion failure at an interface.
	Silicon interdiffusion	A form of electromigration that leads to contact leakage as silicon migrates out of the contact allowing aluminum to diffuse into the resulting void to form a short to the substrate.

Table 2 continued. Electrical failure mode taxonomy.

Primary Identifier	Failure Mode	Definition
Fatigue	Thermal fatigue	An open circuit resulting from thermal coefficient mismatch or poor bonding.
Hot carrier induced degradation	Charge trapping	Occurs when carriers gain enough energy in the transistor channel to inject into the gate oxide and become trapped.
	Interface trap generation	Occurs when high-energy carriers moving along the channel create electron-hole pairs by collisions near the drain, generating oxide interface traps.
Latch-up	Latch-up	The substrate, the n- or p-well, or the diffusion regions being cross-connected with common base-collector junctions.
Mask defects	Mask defects	Extra or missing material in one of the conductive, semiconductive, or insulating layers.
Noise	Alpha particle induced soft errors	Alpha particle(s) strike storage node(s) and alters the memory state.
	Common impedance coupling	Return currents inducing a noise voltage if the magnitude of the induced voltage is significant with respect to the voltage levels in the circuit.
	Electric field coupling	A form of electromagnetic interference characterized by a high voltage in close proximity to the receptor that creates an electric field of sufficient magnitude to result in interference in a receptor.
	Electromagnetic pulse (EMP)	The intense electromagnetic wave created by the charge separation and movement within a nuclear detonation causes semiconductor devices within range of the electromagnetic wave to be destroyed.
	Electromagnetic radiation	A form of electromagnetic interference characterized by high frequency waves and a relatively large distance of separation between the source and the receptor.
	Ground bounce	Shifts in the internal ground reference voltage due to output switching or poor ground connections.
	Magnetic field coupling	A form of electromagnetic interference characterized by large currents that produce magnetic fields and interfere with the receptor.
Overstress or Incorrect current magnitude	Electrical overstress (EOS)	Electrical transients induced from electromagnetic radiation, which causes a higher than specified current that generates additional heat.
	Overcurrent	Large magnitude currents that lead to a severe heat buildup.
	Undercurrent	Insufficient current magnitudes that result in reduced device response times or an inoperative component/device.
Punch-through	Punch-through	When the channel length is so small that depletion regions for the source and drain interact to reduce the barrier for electron flow between these two regions.
Voiding	Voiding	An empty space in the die-attach or non-hermetic case.

Table 3. Electrical failure modes listed with causes and effects.

Primary Identifier	Cause(s)	Failure Mode	Effect(s)
Bonding defect	Wafer processing, plastic package outgassing, or epoxy die attach outgassing and bleedout.	Bond pad contamination	Intermetallic growth, bond resistance change, or breakage of the wire resulting in an open circuit.
	Dynamic force of touch-down impact, static force applied after touch-down, ultrasonic energy, or mechanical vibrations before or after bonding.	Bond pad cratering	Reduced strength of the silicon oxide layers under the bond pads.
	Intermetallic growth, Kirkendall voiding, bond pad contamination, corrosion, intermetallic formation, or manufacturing errors.	Bond resistance change	A bond is considered failed open when its resistance is increased by 20 milliohm from its original value.
	Lack of control in die alignment or the latent evaporation of die adhesive solvent can result in too much or too little die adhesive material.	Bondline thickness error	Reduced bonding strengths, an increased stress on the die, or a volume resistivity increase.
	Poor process controls.	Incorrect bond placement	Crossed wires that cause incorrect signal paths or short circuits.
	Contamination, plating defects, or insufficient bonding pressure in tape automated bonding.	Irregular bump size	Inadequate bonding between the metallized tape and some of the bumps.
	Incorrect bonding parameters, poor surface cleaning before bonding, excessive bonding force, or excessive bonding temperature.	Poor bonding	A short between the pad and substrate (in the case of an excessively high bonding force) or an open circuit.
	An oxide layer that forms a non-eutectic bond.	Poor die-attach	Poor and non-uniform thermal conductivity, circuit performance degradation, and ultimately shorts or opens.
Breakdown	An excessive electric field that leads to a breakdown of (i.e. current discharge through) the gas.	Arc discharge	Short circuit.
	An electric field in the presence of a vacuum or critical pressure region.	Coronal discharge	Loss of data, dielectric breakdown, junction short circuits, and cracks (open circuits) between isolated regions.
	The improper application or handling that results in a separation of static charge and then direct conduction or breakdown of intervening air.	ESD (electrostatic discharge)	Dielectric breakdown, junction short circuits and/or cracks (open circuits) between isolated regions, or bridges (shorts) between conductors.
	Defects in the gate oxide such as pinholes or thin spots or a high voltage across the gate oxide such as ESD or EOS that lead to an excessive electric field across the gate oxide.	Gate oxide breakdown	Shorted GD (gate-drain) or shorted GS (gate-source) that result in current leakage.
	An excessive electric field accelerates the electrons in the gas between the contacts and allows current to flow between the contacts thereby heating the cathode.	Glow discharge	Vaporization of the contact metal.
	Poor processing, particulate defects or contaminants in the thin oxide mask, stacking faults in the oxides, or by imperfections in the SiO_2 that result in thinning of the dielectric.	Time dependent dielectric breakdown (TDDB)	Short circuit.
Contamination	Ionic impurities present in the die attach adhesives (such as aqueous extractable chloride and sodium), environment, human contact, processing materials, packaging, soldering residues, photolithography residues, etching residues, molding compound and any die coating or die attach coating enclosed by the encapsulant that introduce mobile ions (mainly Na^+) into the semiconductor device.	Ionic contamination	A change in threshold voltage, Conduction (shorts) between adjacent devices outside the active region of a transistor, threshold voltage shift, direct chemical attack (corrosion), current leakage near junctions, degradation of bonds, leakage current, and open circuits.

Table 3 continued. Electrical failure modes listed with causes and effects.

Primary Identifier	Cause(s)	Failure Mode	Effect(s)
Cracking	Package-induced surface shear stresses, a large difference in coefficient of thermal expansion, the pressure during reflow due to the vaporizing moisture absorbed by the package, moisture ingress that collects at the delaminated surfaces, the concentration of stress on the passivation layer under the TAB bump during bonding, misaligned leads, excessive bonding force, the saw-and-break method of die separation, thermal stresses induced during cooling, thermal cycling, by wave soldering of through hole components, or the bending of leads.	Cracking	Moisture ingress, the formation of additional cracks, corrosion, shorts, die fracture, a loss of adhesion between the molding compound and the chip, reduced strength, and an introduction of stress concentration.
Diffusion	Poor design or processing mask defects that cause missing conducting material on the wire, small spacings between metal conductors on PCBs, processing residues, exposure to humid and/or polluted environments, and scratches.	Electromigration	Accumulation of vacancies that form a void in the metal (causing resistance increase) and ultimately an open circuit or hillock, which causes a short circuit to adjacent or overlying metal.
	The combination of moisture, DC operating potentials, and ions (mainly Cl- or Na+).	Galvanic corrosion	A decrease in strength of the conductor that eventually leads to mechanical failure and an open circuit in the metallization.
	Two different bulk materials in intimate contact at a surface allowing molecules of one material to migrate into the other by diffusion, dissolution of the base metal into the solder, intermetallic formation at the interface, and precipitation of intermetallics in solder joints.	Interdiffusion	Interfacial adhesion, Kirkendall voiding, brittle bonds that can break under vibration or flexing, bond strength degradation, lifting, increased joint electrical resistance, or open circuits.
	An applied force or the chemical and mechanical properties of the interface affect adhesive failure.	Interfacial de-adhesion	Delaminations in laminated composite materials, separation of bonded joints, separation of a die and the attach material, or separation at the interface of a wire bond and the bond pad.
	Poor design or processing mask defects that cause missing conducting material on the contact, small spacings between metal conductors on PCBs, processing residues, exposure to humid and/or polluted environments, and scratches.	Silicon interdiffusion	Voiding along the thinnest point of the contact, an open circuit, contact leakage, or a short to the substrate.
Fatigue	Thermal coefficient mismatch or poor bonding.	Thermal fatigue	Open circuit.
Hot carrier induced degradation	Carriers inject into the gate oxide and become trapped as a result of transistors having inadequate channel lengths or inadequate gate oxide thicknesses caused by poor designs, imperfect fabrication processes, or spot defects.	Charge trapping	Decreased transconductance, increased substrate current, or increased threshold voltage.
	Oxide interface traps that occur as a result of transistors having inadequate channel lengths or inadequate gate oxide thicknesses caused by poor designs, imperfect fabrication processes, or spot defects.	Interface trap generation	Decreased transconductance, increased substrate current, or increased threshold voltage.
Latch-up	Improper design or manufacture that leads to the substrate, the n- or p-well, or the diffusion regions being cross-connected with common base-collector junctions in a CMOS structure on silicon.	Latch-up	Saturation or the power supply being connected across a low resistance path to ground.
Mask defects	Poor design or processing that leads to extra or missing material in one of the conductive, semiconductive, or insulating layers.	Mask defects	Opens, shorts and transistor stuck-on (i.e. shorted drain-source).

Table 3 continued. Electrical failure modes listed with causes and effects.

Primary Identifier	Cause(s)	Failure Mode	Effect(s)
Noise	The radioactive decay of uranium and thorium impurities incorporated in IC packaging materials or cosmic rays.	Alpha particle induced soft errors	Altered memory state.
	Common impedance voltage drops (i.e., the voltage drops across the common return) are significant with respect to the voltage levels of the circuit.	Common impedance coupling	Interference, receptor behaves in an undesired fashion, false internal chip signals, or other functional problems within the circuit.
	A high voltage that produce electric fields in close proximity to the receptor.	Electric field coupling	Interference, receptor behaves in an undesired fashion, false internal chip signals, or other functional problems within the circuit.
	The intense electromagnetic wave created by the charge separation and movement within a nuclear detonation.	Electromagnetic pulse (EMP)	Semiconductor devices within range of the electromagnetic wave are destroyed.
	Unintentional transfer or reception of electromagnetic energy.	Electromagnetic radiation	Interference, false internal chip signals or other undesired behavior in the receptor circuit.
	Poor ground connection, lumped ground pins, or fast output transition times.	Ground bounce	Interference with signal reception or double-clocking.
	Large currents that produce magnetic fields in close proximity to the receptor.	Magnetic field coupling	Interference, receptor behaves in an undesired fashion, false internal chip signals, or other functional problems within the circuit.
Overstress or Incorrect current magnitude	Improper application or handling of an integrated circuit or electromagnetic radiation (such as nuclear radiation, electromagnetic pulses, radar, lightning, and switched transients).	Electrical overstress (EOS)	A higher than specified current that generates additional heat and could ultimately melt the junctions causing open circuits or short circuits.
	Overloading or shorts.	Overcurrent	A severe heat buildup that can lead to an open circuit in the conductor or a fire induced by overheating materials surrounding the conductor.
	A conducting medium at an excessively low temperature (which decreases electron velocity) or a discharged power source.	Undercurrent	Reduced device response times or an inoperative component/device.
Punch-through	Manufacturing defects and poor design that lead to a very short channel length.	Punch-through	Shorted DS (drain-source).
Voiding	The oxidation of bonding surfaces or when the rate of change of temperature is faster than the permeation rate of the water in the gel.	Voiding	Increase in junction temperature, die attach cracking during temperature cycling, or corrosion.